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The New Topology of Multi Level Inverter with Minimum of Switches

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ABSTRACT— A new multilayer inverter topology is proposed in this study. The cascaded feature is used in this innovative topology. In addition to the isolated DC sources seen in Cascaded H-bridge. The clamping diode in Diode and the multilevel inverter (CHB-MLI) Inverter with Clamped Multilevel (DC-MLI). With these advantages, an inverter topology with 18 total component counts when coupled had been discovered. This proposed topology has the potential to generate up to According to the ratio allocated to its DC sources, there are 17 output levels. Aside from increasing the number of output voltage levels, this study has a relatively low number of component counts. The THD limit defined by IEEE standard is also a goal (i.e. 5 percent) all voltage applications under 69kV.To ensure that the suggested topology is functional, it is being simulated in Matlab/Simulink with various modulation indexes. The amount of THD, the number of voltage outputs, and the RMS voltage are all being monitored and discussed. Finally, to assess the uniqueness of the suggested topology, a comparison study with recently disclosed topologies is being carried out.

KEYWORDS- Topology, THD, multi-level Inverter, DC.

I. INTRODUCTION

In the power business, the multilevel inverter (MLI) is crucial [1]. It's commonly utilised in medium- to high-voltage applications such high-voltage DC transmission, flexible AC power transmission systems (FACTS), renewable energy integration, and high-power drives [2]-[10]. The main purpose of an inverter is to generate AC output from an AC input. With the introduction of the 3-level inverter, the technology took off. This inverter can generate three levels of output voltage (+V, 0V, and –V) in a quasi-square waveform with varying amplitude and frequency. To reduce total harmonic distortion (THD), it must be operated at very high frequencies, resulting in increased switching losses, high dv/dt, voltage doubling effect, and electromagnetic interference. A power output filter as well as a step-up transformer are required to increase the quality of the output voltage waveform. The first MLI was introduced in the 1970s as a result of the aforementioned restrictions. MLI successfully enhances the number of output levels when compared to a 3-level inverter. Furthermore, it has improved the voltage output quality, allowing the output filter's reliance to be lowered or abolished. Furthermore, because a high switching frequency is no longer required, switching loss could be decreased. The CHBMLI is the first MLI, and it uses cascaded features and isolated DC. It is made up of a single cell called an H-bridge cell. By cascading more H-bridge cells, a higher voltage level might be easily reached. This resulted in greater component counts and an isolated DC source, limiting the application's flexibility. DCMLI is introduced later in the 1980s. It divides the voltage source into two portions using a capacitor, with the neutral point in the middle. The clamping diode aids in the voltage step induction. However, employing a capacitor link will result in voltage balancing issues. In later years, the Flying Capacitor MLI (FCMLI) was developed in the hopes of overcoming the limits of DCMLI and CHBMLI [12]-[13]. To produce a voltage step, FCMLI uses the same clamping approach as DCMLI. FCMLI has successfully eliminated the use of isolated DC sources and clamping diodes, according to [12]-[13]. As a result, the application's flexibility was limited by higher component counts and an isolated DC supply. Later in the 1980s, DCMLI is launched. It uses a capacitor to divide the voltage source into two parts, with the neutral point in the middle. The voltage step induction is aided by the clamping diode. Using a capacitor link, on the other hand, will cause voltage balancing concerns. The Flying Capacitor MLI (FCMLI) was created subsequently in order to overcome the limitations of DCMLI and CHBMLI [12]-[13]. FCMLI uses the same clamping method as DCMLI to create a voltage step. According to [12]-[13], FCMLI has successfully removed the use of discrete DC sources and clamping diodes. The constraints of traditional MLI are I an increase in component counts as the desired voltage level grows, resulting in a larger system size and higher

inverter manufacture costs, and (ii) a problem with voltage balancing. Because of this flaw, research on MLI continues to be conducted to this day. The cascaded feature has become well-known among experts in this field. For example, [1], [14], and [16] showed a variety of topologies with cascaded features. The topologies in [14]-[16] are separated into two parts: generation and inversion bridge. In comparison to the traditional MLI, an inversion bridge is made up of a single unit of H-bridge cell and is responsible for setting the polarity of the voltage output. They have also succeeded in improving the quality of the voltage output. Nonetheless, as the number of output levels grows, so does the number of components, especially with the inclusion of an extra inversion bridge. Furthermore, unlike [1], which relied on a DC capacitor link rather than isolated DC sources, the topologies in [14]-[16] make use of the benefits of isolated DC sources. As a result, the voltage balancing approach can be avoided. Despite the fact that voltage balancing is a key flaw in DCMLI, numerous approaches have been provided in [17]. According to [17], voltage balancing could be enhanced by fine-tuning the modulation approach and incorporating an additional voltage balance circuit. The requirement for a three-phase structure is also a drawback to adopting DCMLI. The DCMLI 5-level and 7-level are utilised to feed the inside permanent magnet synchronous motor in [18]. The total number of switches required to create the aforementioned voltage levels is 24 switches and 36 switches, respectively. In addition, an output filter is utilised to increase the THD %. The THD % for DCMLI is better than the cascaded MLI, according to comparison research of 5-level cascaded MLI and DCMLI discussed in [19]. In addition, [20] presents a modified DCMLI. Unlike the standard DCMLI structure, the proposed topology is only created in one phase in [20]. As a result, the number of switches has been greatly reduced. However, adding an additional output filter increases the system's size, and voltage balancing becomes more difficult as the voltage is increased. As a result, the virtues of this topology may be fully exploited if the constraints of CHBMLI and DCMLI could be addressed [21]-[22]. The cascaded feature and isolated DC sources from CHBMLI, as well as the clamping diodes in DC-MLI, are used in the innovative topology suggested in this study. The proposed architecture might create up to 17 levels using 10 switches, 4 diodes, and 4 isolated DC sources when these features are combined. The work is organised as follows: Section II has an overview of the suggested topology, Section III contains operation details, Section IV contains data analysis, and Section V contains a comparison study.

II. CONFIGURATION

Figure 1 depicts the proposed topology's fundamental configuration. This design typically consists of ten switches, four diodes, and four separated DC sources. The toggles Upper legs (S1, S2, S5, and S6) and lower legs (S1, S2, S5, and S6) Legs that are shorter (i.e., S3, S4, S7, and S8). These switches have to be turned on. To avoid a short circuit, they must work in tandem.

Part A and Part B are the two components of the overall structure. Each part generates its own voltage train based on the voltage ratio that has been allotted to it. Each component is designed to seem like a single-phase DC-MLI and is coupled using "floating switches," S9 and S10. The clamping diodes (D1, D2, D3, and D4) act as voltage dividers, causing a higher voltage level to be induced. (1) determines the number of voltage output levels as follows: fig1.

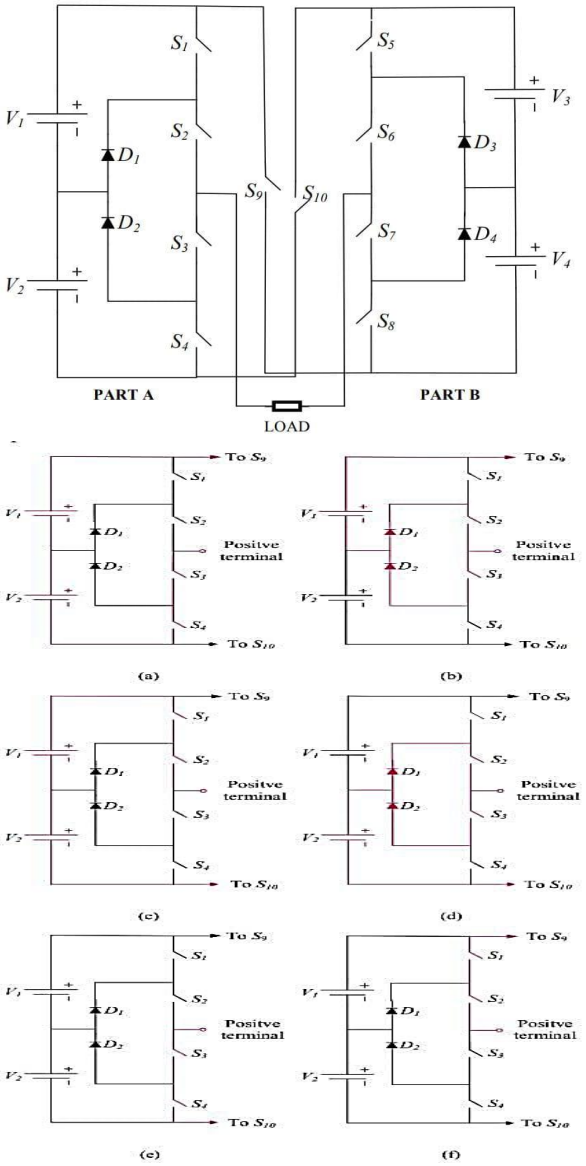


Figure 1: Different voltage variants to design the switches

$$n=2h+1$$

where n denotes the number of voltage output levels and h denotes the total of all voltage ratios in the topology. Every part's switching operation can be classified into four modes. The switching process for Part A was depicted in Figures 1(a) to 1(f).

Each section has five different switching modes: (V1 + V2), V1, 0, (-V2 + (-V1)), and -V1. The positive cycle of voltage waveform production is represented by the switching modes in Fig. 1(a) and Fig. 1(b). S1, S2, and S10 are all turned on in Fig. 1(a) to allow voltage to pass via both DC sources. Complimentary, S3, S4, S9, and S10 must be turned off. Meanwhile, S2, S3, and S10 are turned on in Fig. 1(b). The clamping diode will allow voltage to flow, halving the total DC sources in Part A. Complimentary, S1, S4, and S9 must all be disabled. The identical technique applied to the switching mode in Fig.

1(c) and Fig. 1(d), but the voltage flowed from the negative terminal to the positive terminal during the negative cycle. In the zero state, the switches are turned on to prevent any voltage from flowing through any voltage source. As shown in Fig. 1(e) and Fig. 1(f), there are two alternative switching modes for zero states (f)The sum of the switching modes in Parts A and B will produce the switching states required for each setup. It should also be noted that depending on the ratio allocated to each portion, the suggested topology in Fig. 1 might yield 9, 13, or 17 voltage output levels. Section III will go through this in further detail.

III. DETAILS OF THE OPERATING SYSTEM

for this setup. This arrangement might yield output levels of up to 17 levels when using (1). Part A and Part B have voltage trains of +2VDC, +VDC, 0, -VDC, and -2VDC, whereas Part B has voltage trains of +6VDC, +5VDC, +4VDC, +3VDC, +2VDC, +VDC, 0, -VDC, -2VDC, -3VDC, -4VDC, -5VDC, and -6VDC. Table 1 shows the various switching states.

Table 1: Switching state for 1:3 Configuration

State level	S_1	S_2	S_9	S_5	S_6	V_{ab}
1	1	1	0	0	0	$+8V_{DC}$
2	0	1	0	0	0	$+7V_{DC}$
3	0	0	0	0	0	$+6V_{DC}$
4	1	1	0	0	1	$+5V_{DC}$
5	0	1	0	0	1	$+4V_{DC}$
6	0	0	0	0	1	$+3V_{DC}$
7	1	1	0	1	1	$+2V_{DC}$
8	0	1	0	1	1	$+1V_{DC}$
9	1	1	1	0	0	0
10	0	1	1	0	0	$-1V_{DC}$
11	0	0	1	0	0	$-2V_{DC}$
12	1	1	1	0	1	$-3V_{DC}$
13	0	1	1	0	1	$-4V_{DC}$
14	0	0	1	0	1	$-5V_{DC}$
15	1	1	1	1	1	$-6V_{DC}$
16	0	1	1	1	1	$-7V_{DC}$
17	0	0	1	1	1	$-8V_{DC}$

IV. ANALYSIS OF DATA

Matlab/Simulink R2019a is being used to run the simulation. The suggested topology's rated voltage is capped at 240V. The system is loaded with a 277.6 and 0.55H The operation of each configuration of the proposed topology will be explained in this section. As previously stated, based on the specified ratio, each configuration will yield a varied number of voltage output levels. The topology is used in this study with a 1:1, 1:2, and 1:3 ratio. 1st Configuration: 1st Configuration: 1st Configuration: 1stThe symmetry configuration is defined as V1=V2=V3=V4=VDC, where V1=V2=V3=V4=VDC. This arrangement can create up to 9 levels of output voltage from (1). Each component generates a voltage train of +2VDC, +VDC, 0, -VDC, -2VDC. Table 2 shows the various switching states.

Table 2: state level variations

State level	T1	T2	T9	T5	T6	Vab
1	1	1	0	0	0	+4Vdc
2	1	1	0	0	1	+3Vdc
3	0	0	0	0	0	+2Vdc
4	0	0	0	0	1	+1Vdc
5	0	0	0	1	1	0
6	1	1	1	0	1	-1Vdc
7	0	0	1	0	0	-2Vdc
8	0	0	1	0	1	-3Vdc
9	0	0	1	1	1	-4Vdc

Configuration B. 1: 2

The DC source in Part B is doubled the voltage in Part A (i.e., asymmetry configuration), with V1=V2=VDC and V3=V4=2VDC for this setup. This arrangement can create voltage up to 13 levels of voltage output when using (1). Part A's voltage train is +2VDC, +VDC, 0, -VDC, and -2VDC, whereas Part B's voltage train is +4VDC, +3VDC, +2VDC, +VDC, 0, -VDC, -2VDC, -3VDC, and -4VDC. Table 3 depicts the switching stage.

Table 3: Switching state for 1:2 configuration

State level	S_1	S_2	S_9	S_5	S_6	V_{ab}
1	1	1	0	0	0	$6V_{DC}$
2	0	1	0	0	0	$5V_{DC}$
3	0	0	0	0	0	$4V_{DC}$
4	0	1	0	0	1	$3V_{DC}$
5	0	0	0	0	1	$2V_{DC}$
6	0	1	0	1	1	$1V_{DC}$
7	0	0	0	1	1	0
8	0	1	1	0	0	$-1V_{DC}$
9	0	0	1	0	0	$-2V_{DC}$
10	1	1	1	0	1	$-3V_{DC}$

Configuration C. 1: 3

Part B's DC source value is tripled compared to Part A's, with V1=V2=VDC and V3=V4=3VDC resistive and inductive load, respectively. Modulation index m equal to 1.0, 0.8, 0.5, and 0.3 is used in the simulation. The goal of modelling it with various modulation indexes is to see how

Table 4: Result obtained from 1: configuration

m	Number of level, n	THD, %	V_{RMS}, V
1.0	9	9.44	171.8
0.8	7	12.26	133.9
0.5	5	17.63	88.03
0.3	3	32.12	48.03

Table 5: Result obtained from 1:2 configuration

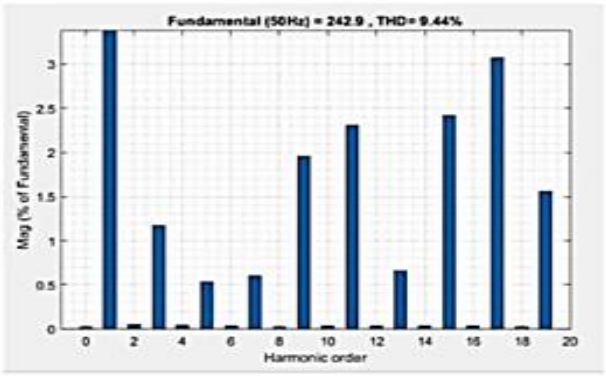
m	Number of level, n	THD, %	V_{RMS}, V
1.0	13	6.44	170.70
0.8	11	8.78	136.30
0.5	7	12.30	86.60
0.3	5	22.24	53.04

Table 6: Result obtained from 1: 3configuration

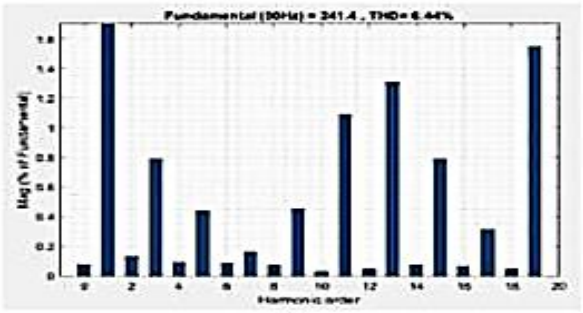
m	Number of level, n	THD, %	V_{RMS}, V
1.0	17	4.90	170.20
0.8	14	6.29	136.40
0.5	9	9.44	85.99
0.3	6	15.72	53.20

modulation index affects the number of voltage output levels and the THD % of the suggested topology. The outcomes of the 1:1, 1:2, and 1:3 configurations are shown in Tables 4, 5, and 6, respectively. These statistics concluded that when the modulation index increases, the number voltage drops. Meanwhile, when the modulation index rises, the THD % rises. However, the variation in THD percentage is not only due to the modulation index. THD percentage when m=0.5 for a 1:3 configuration, for example, is higher than the value in 1:2 and 1:1 configuration. Each of these setups has a distinct number of output voltage levels when m=0.5. As a result, it can be deduced that the THD percentage is likewise affected by the number of voltage output levels. The higher the number of voltage levels, the better the MLI in terms of THD quality. Nonetheless, the THD percentages derived from these topologies are almost identical to the IEEE Std 519-1992 THD acceptable norm. The permissible THD limit for applications below 69kV is 5%, according to this specification. The THD of the 1:3 arrangement is within the intended work. allowable limit but 1:1 configuration and 1:2 configuration might require filter to further reduce the THD percentage.

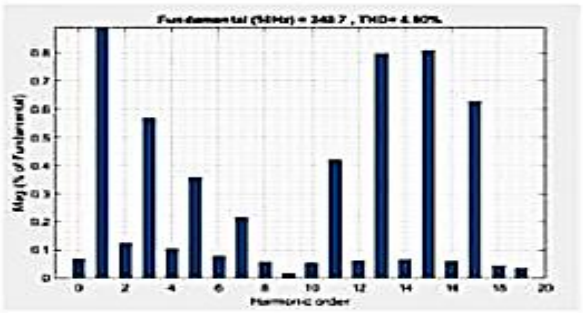
The modulation index has no effect on the amplitude of the output voltage VRMS. There is a small amount of variation in the VRMS value for different voltage levels, but it is not substantial. As a result, the number of voltage levels has no effect on the VRMS. The DC offset that occurs during simulation could be the cause of the divergence. Figures 2(a), 2(b), and 2(c) show the harmonic spectrum for the 1:1, 1:2, and 1:3 configurations, respectively, when m is equal to 1. (a)



(a)



(b)



(c)

Figure 2: Modulation levels

The offset value could be detected at harmonic order equal to zero from Fig. 2(a) to Fig. 2(c). The smaller the value of fundamental voltage, the larger the offset value. Figures 3(a), 3(b), and 3(c) show the comparisons for the aforementioned designs in terms of the number of output voltage levels, respectively. (a)

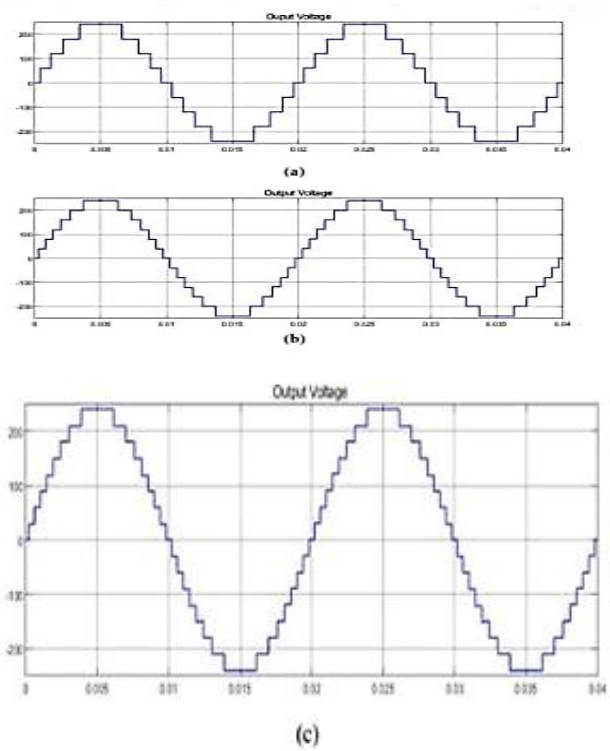


Figure 3: Voltage output for (a) 1:1 configuration, (b) 1:2 configuration, and (c) 1:3 configuration

The summary comparison for these configurations in term number of level output and THD percentage are illustrated in Fig. 4 and Fig. 5.

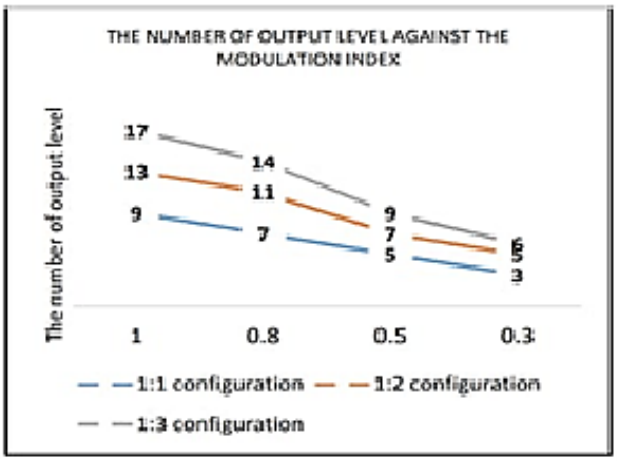


Figure 4: Number of voltage level against the modulation index

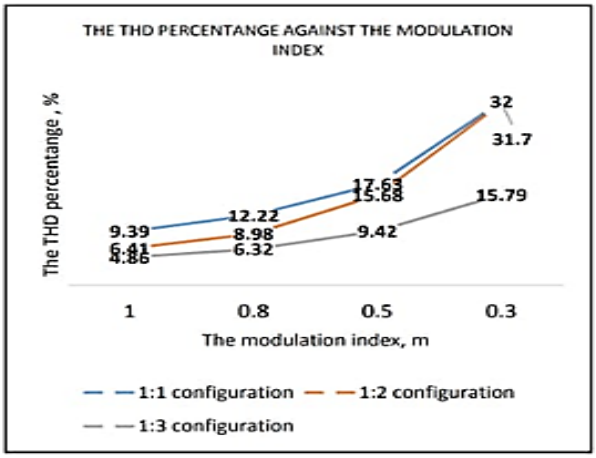


Figure 5: Number of THD percentage against the modulation index

Furthermore, the voltage stress across the switches will be unequal because the switches are coupled to various voltage sources. As a result, the amount of power shared by the switches, as well as the amount of power lost at the switches, will vary.

V. COMPARATIVE RESEARCH

The proposed topology is compared to the topologies proposed in [1], [13], and [20] in this section. To determine the polarity of the voltage output, topologies [1] and [4] used a cascaded feature with an inversion bridge. In contrast to [1,] the design in [13] splits the voltage source using a capacitor. In the meantime, the topology in [20] is DCMLI's updated structure. Only one DCMLI phase is used in this topology. When only one phase is used, the number of components is greatly reduced. Table 8 compares the suggested topology to the topologies in [13] and [20] for generating 9-level voltage output. Table 7 shows that topology [13] has fewer component counts than the suggested topology, but the THD is about treble that of the proposed topology. Meanwhile, due of the presence of an output filter, the THD percentage for topology [20] is within the acceptable THD limit (i.e., 5%). If the suggested topology includes a filtering element at the output, it will almost likely achieve the same THD percentage as [20].

Table 7: Compare between proposed topology and Cascade MLI

Parameters	Proposed Topology	Cascaded MLI in [1]
No.of sources	4	1
No.of switches	10	14
No.of diodes	4	9
No.of capacitors	0	10
Total component counts	18	34
No.of voltage level	17	21
THD (%)	4.90	3.93

Table 8: Parameter of Proposed Technology.

Parameters	Proposed Topology	Cascaded MLI In [13]	Modified DCMLI in [20]
No. of sources	4	4	1
No. of switches	10	11	10
No. of diodes	4	0	4
No. of capacitors	0	0	6
Total component counts	18	15	20
THD (%)	9.44	25.66	1.31 (with Filter)

Meanwhile, Table 8 compares the suggested topology to the architecture in [1] in order to generate a 17-level voltage output waveform.

Table 8 shows that the number of components required to create the 21-level output voltage in [1] is nearly double that of the suggested design. Despite the fact that [1] has a greater output voltage, the THD difference between it and the suggested topology is not significant. In fact, assuming the same difference in output voltage level that may be produced, the THD gap between the 1:2 and 1:3 configurations described in this study is 1.54 percent, which is higher than the THD gap between the 1:3 configuration and topologies presented in [1], which is just 0.70 percent.

VI. CONCLUSION

Based on the simulation results, it can be stated that the proposed topology is capable of solving the difficulty that conventional multilevel inverters confront. This proposed architecture achieves a high level of output while using a small number of total components. As a result, the proposed topology could yield a low THD % and so improve the system's quality. Furthermore, a comparative investigation revealed that the proposed topology outperforms the competition in terms of THD output and total component counts. Although the THD percentages for 1:1 and 1:2 configurations are slightly higher than the permitted limit, the output filter could improve them. The presence of the output filter will undoubtedly raise the system's size, but not its number.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

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