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Design and Implementation of Two Speed Multiplier Using FPGA

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ABSTRACT- Multiplication has recently been given top priority in all applications of digital signal processing and machine learning. It is crucial to control the area, latency, power, and performance overall using parallel implementations. This will require more logic sizes with critical routes and more power consumption because the amount of multiplications will also result in a number of arithmetic additions and subtractions. In order to address this issue, the proposed work will present extensive optimization of radix-4 multiplication circuits using a modified booth algorithm and a kogge stone adder, which will result in smaller critical paths and improved performance overall when compared to Wallace trees and DADDA multipliers. Finally, this effort will synthesize in a Xilinx FPGA using Verilog HDL and demonstrate area comparisons.

KEYWORDS- FPGA, Verilog HDL, DADDA multipliers, DFT, DCT

I. INTRODUCTION

Frequency transformations like DFT, FFT, and DCT, as well as frequency domain filtering (FIR, IIR) [1], are tasks that must be completed by digital signal processing. Multiplication is a crucial hardware component for this function. As a result, an important factor in deciding how well the system as a whole performs is the multiplier's performance. This is due to the multiplier being the system component that operates slowly and takes the longest. As a result, the multiplier speed and area optimization presents a significant challenge to system designers.

Today's digital signal processing and a number of other applications rely heavily on multipliers. Numerous academics have attempted and are attempting to create multipliers with one of the following design goals: fast speed, low power consumption, or regularity of layout.

II. LITERATURE SURVEY

"An effective Carry Select Adder design by Common Boolean logic SQRT architecture", Due to the growing demand for portable systems, area occupancy is essential in integrated circuit design. One of the fastest adders, the Carry Select Adder (CSLA) [2], is employed in several data-processing processors to carry out quick arithmetic operations. This study proposes a common Boolean logic term-shared carry select adder that is space-efficient. One XOR gate, one inverter gate, one AND gate, and one inverter gate are all that are required for each summing operation after logic simplification and sharing partial circuits. The multiplexer selects the appropriate output based on the logic states of the carry in signal.

Recently, approximate computing has become known as a viable method for designing digital systems in an energy-efficient manner. Many systems and applications must be able to tolerate some loss of quality or optimality in the computed result in order for approximate computing to work. A significant increase in energy efficiency is made possible by approximation computing approaches, which remove the requirement for totally accurate or fully deterministic operations. The design of approximation arithmetic blocks, relevant error and quality measurements, and algorithm-level strategies for approximate computing are all covered in this paper's survey of current developments in the field.

Anab Rashid et al. [4] describe an effective algorithm technique to find the maximum gains for the controllers is the best option. The gains of the controllers are addressed in this work and thus are optimized using a meta-heuristic technique in this study.

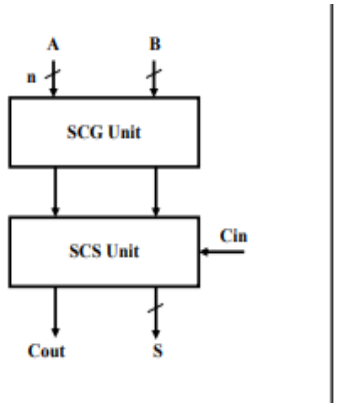
III. EXISTING SYSTEM

Given that it determines the execution space, execution time, and overall performance of parallel implementations, MULTIPLICATION is perhaps the most crucial basic for digital signal processing (DSP) and machine learning (ML) applications [3]. The improved Booth algorithm at larger radixes in conjunction with Wallace or Dadda tree has typically been considered as the highest performing version for general problems despite the substantial work on the optimization of multiplication circuits. Multiplication is often carried out in one of three ways in digital circuits: 1)

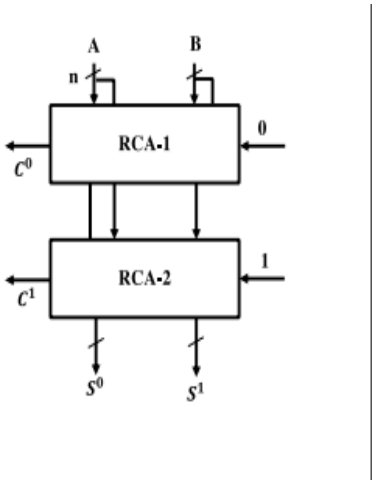
parallel-parallel, 2) serial-parallel (SP), and 3) serial-serial. We investigate an SP two-speed multiplier (TSM) [5] that conditionally adds the nonzero encoded portions of the multiplication and skips over the zero encoded portions using the modified Booth method.Reduced precision representations are frequently utilized in DSP and ML implementations. In this paper, a dynamic control structure is presented to fully remove some computations during runtime. This is accomplished by utilizing a modified serial Booth multiplier that, regardless of position, skips over encoded all-zero or all-one processing. The multiplier is created to be a simple block that is readily implemented into existing DSPs, CPUs, and GPUs. It takes all bits of both operands in parallel. The multiplier significantly improves computational performance for specific input sets. The fact that the multiplier's performance is enhanced by both input set sparsity and its internal binary representation is one of its important features.

IV. CARRY SELECT ADDER

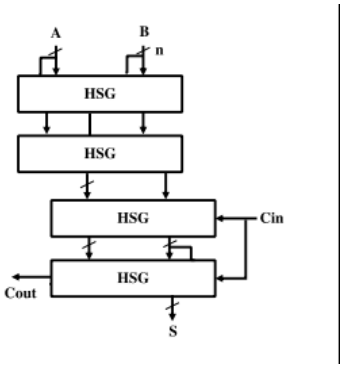
According to Figure 4, the traditional CSLA has a single sum, carry generation unit and sum, and carry selection unit. Two ripple carry adders, one with carry input zero and the other with carry input one, can be used to create a sum and carry generation unit, as illustrated in Figure 5. N is the adder bit width, where. Utilizing the half-sum generator (HSG), half-carry generator (HCG), full-sum generator (FSG), and full-carry generator (FCG) (illustrated in Figure 6), an nbit RCA can be created. The RAC-RAC-2 and I produce n-bit sums (S0 and S1) and carry out (C0out and Clout), which are equivalent to input-carry (Cin=0 and Cin=1), as shown in below diagram respectively.



(a)



(b)



(c)

Figure 1 (a) (b) (c): Logic expression of BEC-based CSLA

BEC-based CSLA consists of binary to excess-l converter in the place of RCA-2 in conventional CSLA. The RCA is same as that of RAC-l in the conventional CSLA; it calculates n-bit sum {s0 1 (i)} and carryout {C0 out} corresponds to Cin = 0. Inputs to the BEC unit is {s0 1 (i), CO out} and output is (n+ 1)-bit excess-l code.

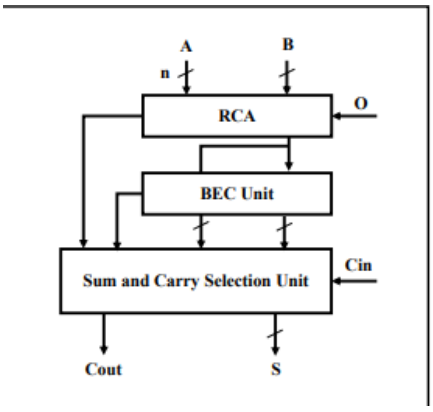


Figure 2: Output

V. CONCLUSION

In this study, we proposed a TSM that is split into two separate sub circuits, each of which has a distinct critical

path. The distribution of the bit representation is the only factor that can be changed to enhance this multiplier's performance in real time. We demonstrated how typical compute sets, like uniform, Gaussian, and neural networks, may anticipate significant gains of 3 and 3.56 using traditional learning and sparse approaches, respectively, for bit widths of 32 and 64. When compared to the standard parallel multiplier, the cost of handling representations with smaller bit widths, like Gaussian-8 on a 16-bit multiplier, is reduced and shows up to a 3.64 improvement. Future research will concentrate on methods for developing apps that fully utilize the two-speed optimization.

CONFLICTS OF INTEREST

The authors declare that they have no conflicts of interest.

REFERENCES

[1] Li, Y. Zhai, and X. Li, "A fast Huffman Decoding Algorithm For Image Compression," in Proceedings of the IEEE International Conference on Big Data Computing and Communication Systems, 2020.

[2] Information Technology, “Generic Coding of Moving Pictures and Associated Audio Information”, Part 2: Video, Standard ISO/IEC 13818- 2:2013, 2019.

[3] Alistair Moffat, 2019, “Huffman Coding”, ACM Computer Survey, 52, 4, Article 85, August 2019.

[4] Anab Rashid , Satish Saini, Sheikh Safiullah, Zahid Farooq. “System Dynamics and Frequency Regulation of a Multi-Area Power System Using an Optimal Controller”, International Journal of Innovative Research in Engineering & Management (IJIREM), 9, no.3, pp. 66-72 (2022), doi:10.55524/ijirem.2022.9.3.9.

[5] Liu, Yue, and Li Luo. "Lossless Compression of Full-Surface Solar Magnetic Field Image Based On Huffman Coding." In 2017 IEEE 2nd Information Technology, Networking, Electronic and Automation Control Conference (ITNEC), pp. 899-903. IEEE, 2017.