Floating Gate MOSFET Based Differential Amplifier and Impact of Body Bias

J. Jenifer Majella, R. Ambika

Abstract- **In this work, a floating gate MOSFET (FGFET) based single-ended differential amplifier with current mirror active load is designed and analyzed along with the body bias. The input transistors of the differential block are constructed using FGFET. The floating gate voltages and the body voltages are used to change the device characteristics and there by the amplifier characteristics.**

***Index Terms*- Differential amplifier, Floating gate MOSFET, Body bias, Threshold Voltage shift**

I. INTRODUCTION

Traditionally Floating gate (FG) transistors are used in flash memories and EEPROM devices [1]. In the last few years, FG MOSFETs are being utilized in a number of new and exciting analog applications. These devices are available in standard CMOS technology because they are being widely used in digital circuits. Floating gates offer dynamic threshold voltage devices. This property is being exploited widely in analog applications. The body bias of the conventional MOSFET also offers threshold voltage tuning to some extent. Even though both of these effects have already been studied in the literature, the combined effects of these are yet to be investigated. In this paper, FGFET based differential amplifier with body bias is proposed to obtain tunability and programmability. In the next section, the simulation methodology is presented. The simulation results are presented in Section III followed by conclusion in section IV.

II. SIMULATION METHODOLOGY OF FGFET

A. FGFET model and simulation

The presence of the trapped charges in the floating gate results in the variation of the threshold voltage thus providing tunability [8]. The voltage across the floating gate is given by the equation,

$$V_{FG} = \sum_{i=1}^{N} [(C_i/C_T)V_i+(C_{GS}/C_T)V_S+(C_{GD}/C_T)V_D+(Q_{FG}/C_T)]$$

$$= \sum_{i=1}^{N} [(C_i/C_T)V_i+(C_{GD}/C_T)V_{DS}+(C_{GB}/C_T)V_{BS}+(Q_{FG}/C_T)+V_S]$$

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J.JENIFER MAJELLA, ECE, SSN college of Engineering, Chennai, Tamilnadu, India.

R.AMBIKA, ECE, SSN college of Engineering, Chennai, Tamilnadu, India.

The equations that model the static, large signal behavior of an FGMOS can be obtained by combining a standard MOS model for the same technology with the equation that relates V_{FG} to input voltage (*Vi)*, drain voltage (V_D), source voltage (V_S), input capacitance (C_i), gate to drain capacitance (C_{GD}), gate to source capacitance (C_{GS}), gate to body capacitance (C_{GB}) and the floating gate charge (Q_{FG}). This equation can be obtained by applying the charge conservation law to the floating node (FG) [8].

The term C_T in the above equations refers to the total capacitance seen by the FG and is given by,

$$C_{T=} C_{GD+} C_{GS+} C_{GB+} \sum_{i=1}^{N} C_i$$

The corresponding floating gate model is shown in Fig. 1.

Since SPICE cannot accept floating node which has no DC branch to ground, high value resistor is added with each capacitor such that maintaining the same time constant in every branch [8].

130 nm PTM technology file is used in this paper. The I_D-V_G characteristics @ programmed and erased conditions are shown in Fig. 2 for two different body voltages. V_{DD} of 1.3V is used throughout the study. Depending on the voltage applied at Vtune1 the FGMOS is in programmed or in erased condition that in turn changes threshold voltage. Along with this substrate voltage also affects the threshold voltage. The threshold voltage values are tabulated in Table 1.

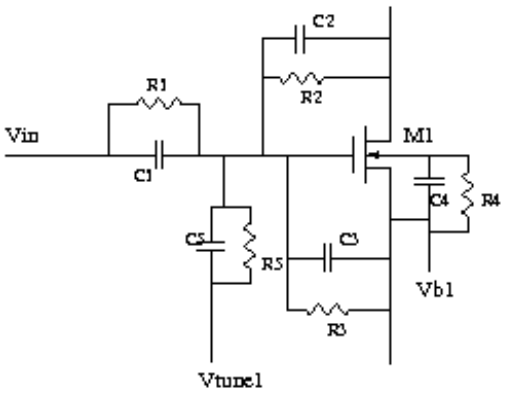

Fig. 1 Model of FGFET

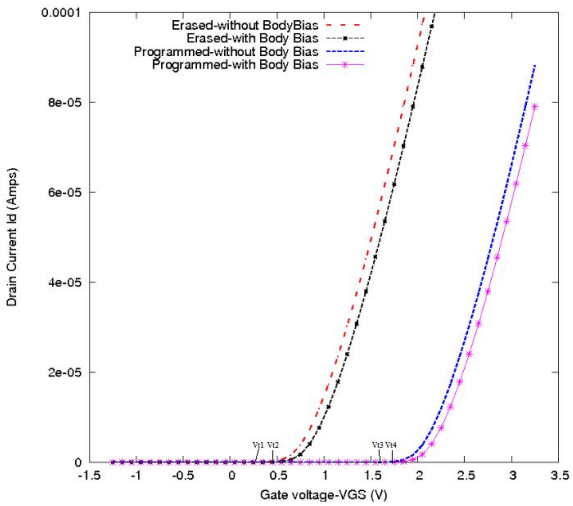

Fig. 2 I_D – V_G Characteristics

Table 1 Threshold Voltage shift

Vtune1	Vb1	Threshold Voltage	Vt
Erased Condition	Zero bias	301.3mV	Vt1
Erased condition	Negative bias	427.5mV	Vt2
Programed condition	Zero bias	1.618V	Vt3
Programed condition	Negative bias	1.72V	Vt4

B. Differential amplifier

A single stage single ended differential amplifier with active current mirror load is shown in Fig. 3 [10]. This is implemented using the FGFET model discussed previously, and is shown in Fig. 4.

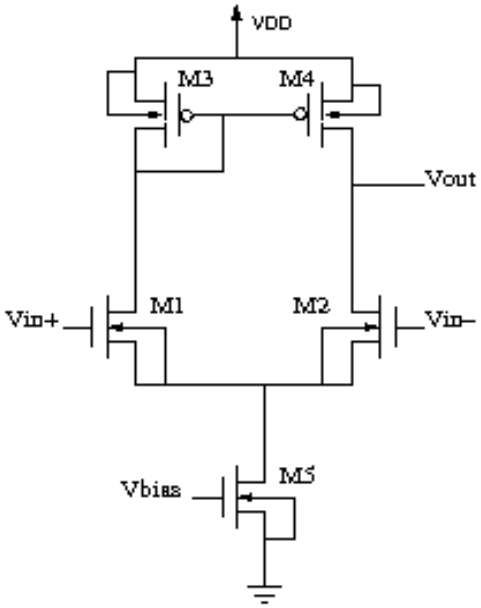

Fig. 3 FGFET based Differential Amplifier

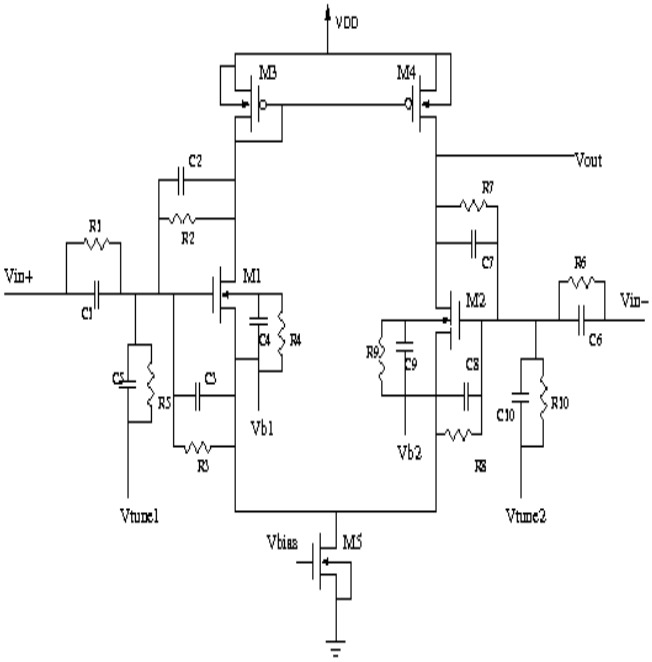

Fig. 4 FGFET based Differential Amplifier

The two input transistors M1 and M2 are implemented using the FGMOS model named FG1 and FG2. Other devices M3, M4 and M5 are the conventional MOSFETs. Vtune1 and Vtune2 are the tuning voltages of FG1 and FG2 respectively. Vb1 and Vb2 are the voltage applied at the body terminal of transistor FG1 & FG2 respectively.

C. Body Bias

If the source and substrate terminals are tied together then the substrate does not have any control on the device. It is possible to apply a voltage the substrate which modifies the threshold voltage of the device. The substrate bias effect (also called body effect) varies the threshold voltage for either type of device [9].

III. RESULTS AND DISCUSSIONS

FGFET transistor based Differential amplifier (shown in Fig. 4) is simulated using 130nm CMOS technology. Both the body voltages (Vb1 and Vb2), and the floating gate voltages are varied and the performance of the differential amplifier has been studied. The studies are done at two levels i.e. one without body bias and the other with body bias. The gain and power of these studies are tabulated in Table 2 and Table 3.

Table 2 Power and gain without body bias

FG1	FG2	Gain	Power(W)
Erased	Erased	3.761	5.536343e-007
Erased	Programmed	0.969	2.867450e-007
Programmed	Erased	1.28	9.154319e-009
Programmed	Programmed	0.250	2.487530e-011

It can be observed from Table 2 that the gain is more if both the FGs are erased and consume high power or alternatively the gain is less if both the FGs are programed and consumes less power. This is because of the threshold voltage variation between erasing and programming.

Table 3 Power and gain with body bias

FG1	FG2	Vb1	Vb2	Gain	Power(W)
Erased	Erased	Zero bias	Negative bias	0.621237	3.760760e-007
Erased	Programmed	Zero bias	Negative bias	0.96969	2.867518e-007
Programmed	Erased	Zero bias	Negative bias	0.054873	9.157766e-009
Programmed	Programmed	Zero bias	Negative bias	0.2515	3.176194e-011
Erased	Erased	Negative bias	Zero bias	4.053598	2.654954e-007
Erased	Programmed	Negative bias	Zero bias	0.00303	8.351070e-008
Programmed	Erased	Negative bias	Zero bias	0.001290	9.193225e-009
Programmed	Programmed	Negative bias	Zero bias	0.25112	3.171061e-011
Erased	Erased	Negative bias	Negative bias	3.878177	1.500600e-007
Erased	Programmed	Negative bias	Negative bias	0.003031	8.351753e-008
Programmed	Erased	Negative bias	Negative bias	0.005538	9.196585e-009
Programmed	Programmed	Negative bias	Negative bias	0.251870	3.856227e-011

Typical differential amplifier parameters like input versus out characteristics, gain versus frequency, common mode gain versus frequency, common mode rejection ration versus frequency are shown in Fig. 5 to Fig. 8 for erased condition. The above figures are shown for two different body voltages (zero bias and negative bias of -1.3 V).

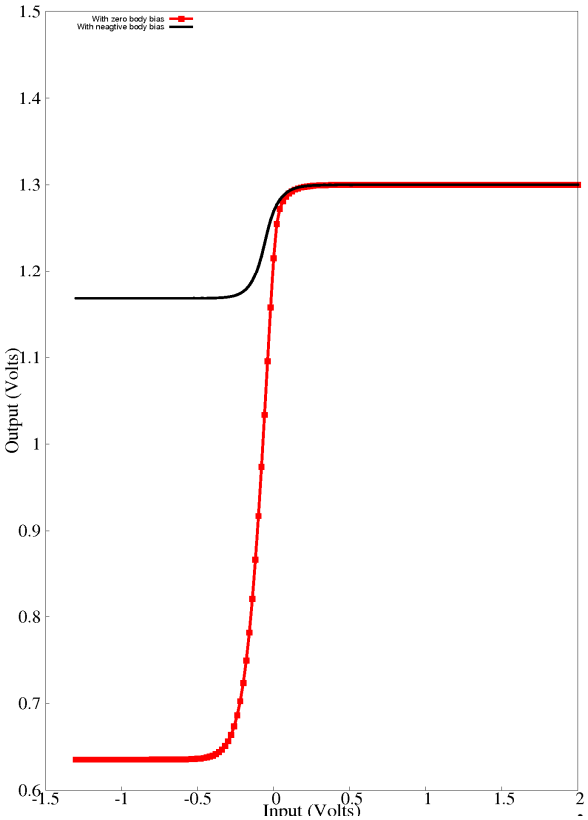

Fig. 5 Input Vs Output characteristics

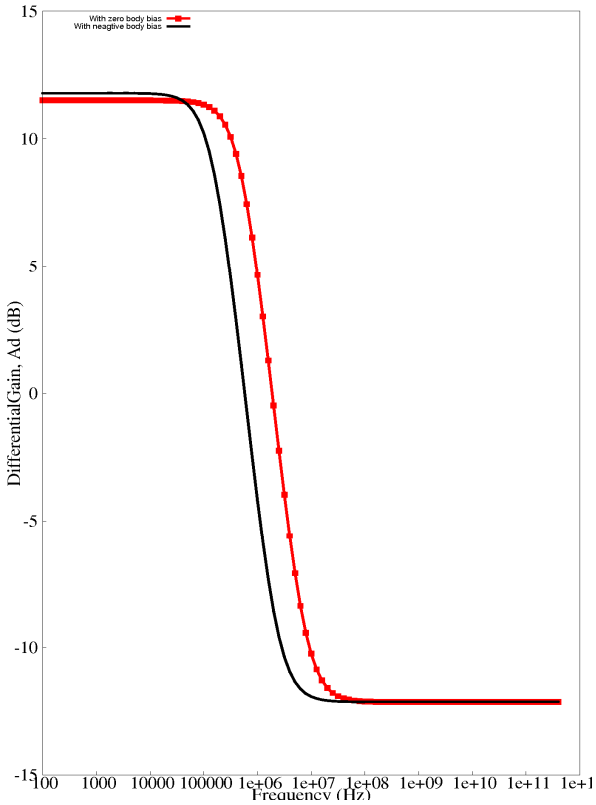

Fig. 6 Differential Gain Vs Frequency

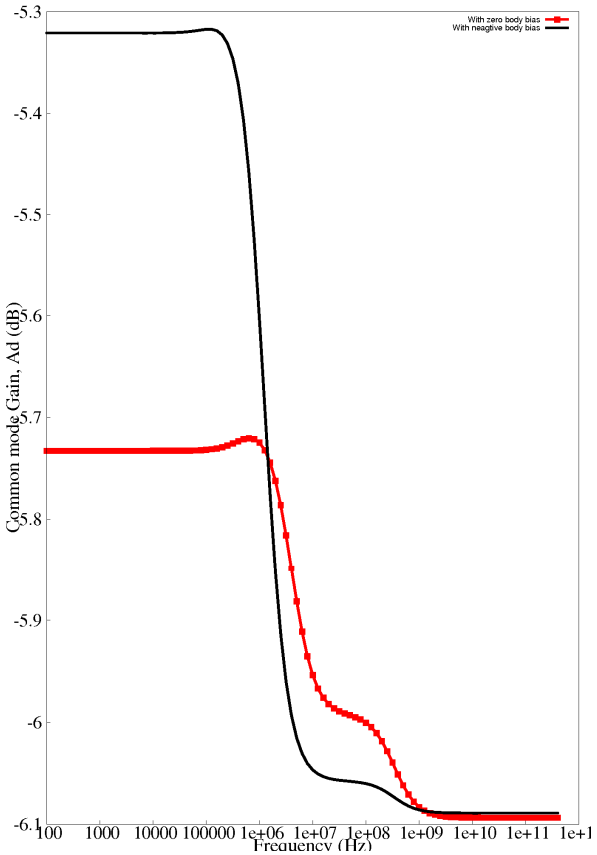

Fig. 7 Common mode Gain Vs Frequency

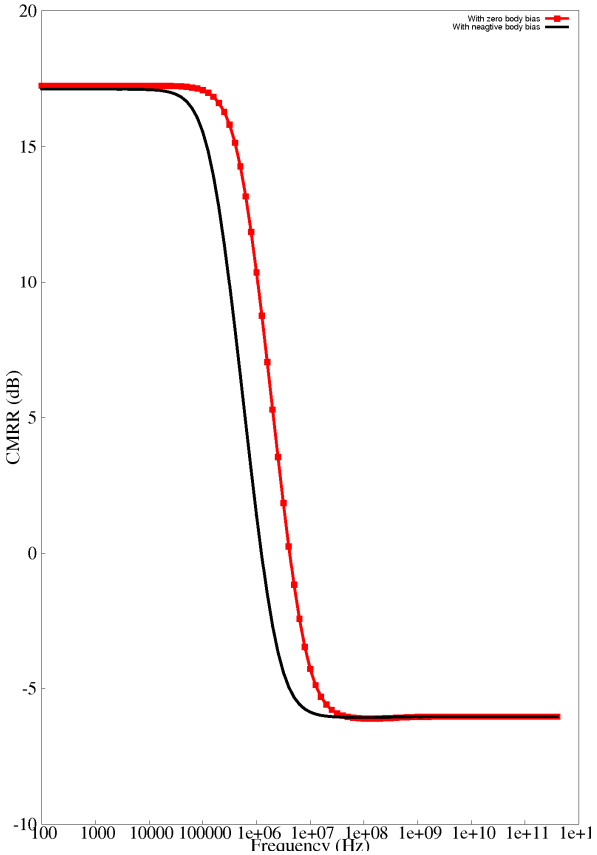

Fig. 8 CMRR Vs Frequency

IV. CONCLUSION

A FGFET-based differential amplifier along with body bias has been studied in this work. Both the floating gate voltage and the body voltage have been used to change the device characteristics and there by the amplifier characteristics.

ACKNOWLEDGEMENT

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