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Implementation of a Fully Automatic Four-way Traffic Light Controller Using Verilog

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ABSTRACT- The traffic control system is one of the challenging problems in metropolitan and developed cities. This is due to the large number of vehicles and the high dynamics of the traffic system. Impoverished traffic systems are the big reason for accidents and time losses. In this project, the Fully Automatic Four-way Traffic light controller is implemented by using Verilog and we have overcome some drawbacks i.e., we included the area detection parameter that improves the detection of vehicles compared to the design part in the base paper.

KEYWORDS- Finite State Machine, Hardware Description Language, Verilog, Xilinix Vivado.

I. INTRODUCTION

Traffic congestion is one of the predominant problems prevailing in cities and towns. In T-intersection and four-way intersections, the probabilities of accidents are slightly higher. So, to ensure smooth flow of traffic and to avoid road accidents, traffic light systems are used.

We designed a traffic light controller system for four-way intersection roads. In this system, the waiting time of vehicles at the intersection is reduced to a great extent. Microcontroller and Microprocessor-based traffic light systems are already present. But the disadvantage associated with these systems is that they work on a fixed time, and don't have flexibility. So, this paper concentrates on developing a reconfigurable traffic light controller system. Verilog is chosen for modeling the traffic light controller system, as usage of Verilog HDL allows the definition of the specifications of the parameters used in the design of the system. Also, Verilog HDL is one of the commonly used HDLs as it has a simple syntax and somewhat resembles software programming languages.

Different types of traffic control systems are put forth by researchers for different real-time situations. A traffic light controller was designed using Verilog HDL considering two roads [1] and a T-junction [2]. A system for four-way intersections was implemented using two signals, red and green [3]. Another system uses three signals, red, yellow, and green to regulate the traffic [4]. However, the drawback of these systems for four-way intersections is that they don't allow the maximum possible movement of vehicles across the intersection [3][4]. Vehicles from a few roads are made to wait at the intersection unnecessarily as allowing them doesn't disturb the moving vehicles. [5]The designed system makes sure that this drawback is removed to allow the maximum transportation of vehicles across the intersection and to prevent unnecessary waiting time for motorists.[5]

Melay model of Finite State Machine (FSM) is used to design the traffic light controller system as the output of the system (traffic light signals) depends only upon the current state of the system.[6] This feature makes the system fully automated. The system considers the four roads to have different traffic and makes use of the Binary encoding scheme.[6] Compared to other works, the proposed system is more efficient by making use of a minimal number of states which are necessary enough to allow the maximum transportation of vehicles across the intersection.[7] The reduction in several states also helps in achieving minimal power consumption. The traffic controller system also makes use of the maximum possible number of safe states. Before the stoppage of traffic across each direction, the yellow signal is displayed in the corresponding displays which indicates that the flow of traffic will be stopped in a few seconds.[7] The states containing yellow signals act as safe states and prevent the possibility of accidents. A Simulation-based system is designed and the same is done using Xilinx Vivado.[8] Complete information on the system design is obtained using various facilities present in this software like utilization reports, power reports, etc.[8]

II. METHODOLOGY

The paper concentrates on developing a traffic light controller system for a four-way intersection with vehicle detection. Each road has three light displays corresponding to the flow of traffic towards the other three roads. Hence there are twelve light displays in total at the intersection. Using a common control logic. This simplifies the design with four light displays. Each of these light displays has the provision to show red, green, and yellow signals. The red signal indicates to stop, the green signal allows the flow of traffic and the yellow signal specifies that the flow of traffic will be stopped in a few seconds. The designed system helps to prevent vehicle collisions at the intersection by the use of 'safe' (yellow state) states. The red, yellow, and green signals of each light display are formed as individual outputs.

III. IMPLEMENTATION OF TRAFFIC LIGHT CONTROLLER SYSTEM

The proposed traffic light controller system is designed to operate at a maximum frequency of 10.0 MHz. The period (T) of the clock used in this system is given by the formula

$$T = 1/f$$

Where f is the maximum operating frequency of the system.

IV. STATE DIAGRAM

The vehicle movement during the S0 and S4 states such as are comparatively higher than that during the other states such as S1, S2, S3, S5, S6, and S7. So, the green signal timing for S0 and S4 states is set to be more than that of other states. The signal timing for two states is set to 16 seconds and for S2 and S6 states, the signal timing is set to 8 seconds, and for S1, S3, S5, and S7, the signal timing is set to 4 seconds. This implies that during the S0 and S4 states, the present state of the displays will continue for 16 seconds and when the time exceeds 16 seconds, the system goes into the succeeding next state. Similarly, in other states, the present status of the displays will continue for 8 and 4 seconds and when the time exceeds 8 and 4 seconds, it moves into the succeeding even state. After the S7 state, the system again enters into the S0 state and this cycle continues. The time taken for the system to complete one full cycle is 64 seconds. Figure 1 illustrates the state diagram of the proposed system.

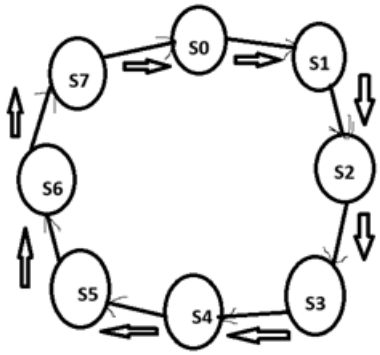

Figure 1: State diagram of the designed system.

V. STATE TABLE

In each of the states, if the bit is 3, it indicates that the light display is showing a red signal, and so, the movement of vehicles in the direction corresponding to the light display is rejected.

Table 1: State table of the proposed system

State	North	East	South	West	No. of Clock cycle
S0	1	3	3	3	16
S1	2	2	3	3	4
S2	3	1	3	3	8
S3	3	2	2	3	4
S4	3	3	1	3	16
S5	3	3	2	2	4
S6	3	3	3	1	8
S7	2	3	3	2	4

Similarly, if the bit is 2, it corresponds to a yellow signal and indicates that the traffic flow will stop soon. If the bit is 1, it corresponds to a green signal, and the flow of traffic in the corresponding direction is allowed. The S1, S3, S5, and S7 states act as 'safe' states as the light displays show yellow signals indicating that the flow of traffic will be stopped soon so that vehicles from those directions can stop, since crossing the intersection during the period of the yellow signal of the current state may lead to accidents due to the flow of traffic regulated during the succeeding S0 and S4 states.

VI. RESULTS AND DISCUSSION

The proposed system is designed as a Melay FSM using Xilinx Vivado and Verilog HDL. Simulation, synthesis, implementation, and bitstream generation were done and no DRC violations were found.

A. Simulation

Figure 2 In the digital symphony of Verilog, the traffic light controller's waveform pirouettes through cycles, orchestrating hues of safety and order are shown in below.

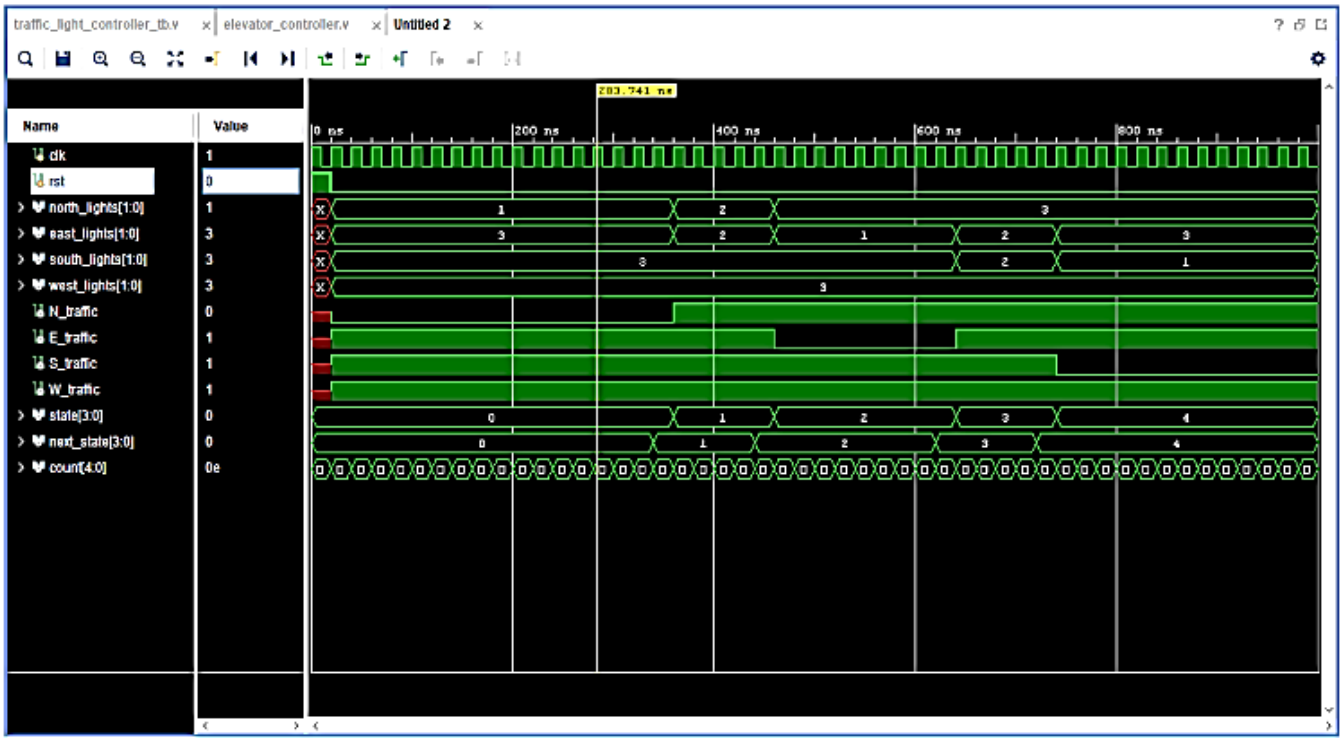

Figure 2. Simulated waveform of the system

B. RTL Schematic

Figure 3 shows the RTL schematic of the designed system

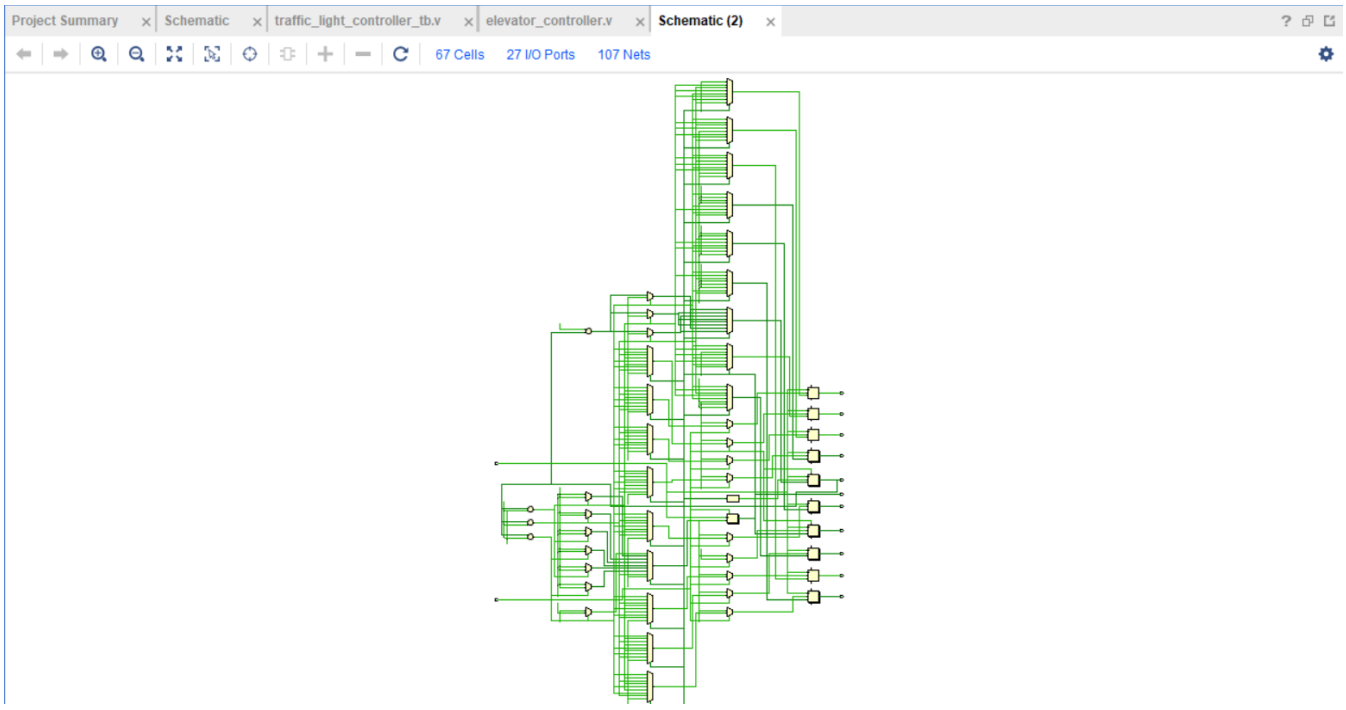

Figure 3: RTL schematic of the system

C. Utilization Report

It was observed that the utilization report generated during synthesis matched with the utilization report generated during implementation. The obtained utilization report is shown in Figure 4.

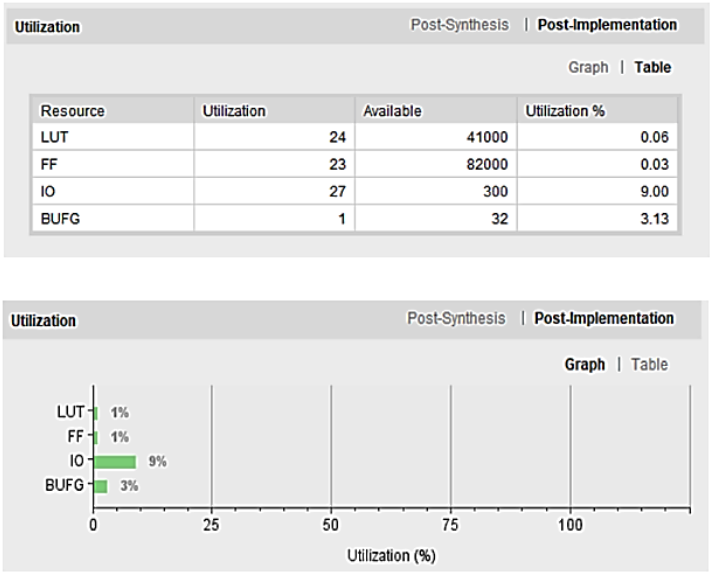

Figure 4 Utilization report of the system

D. Power Report

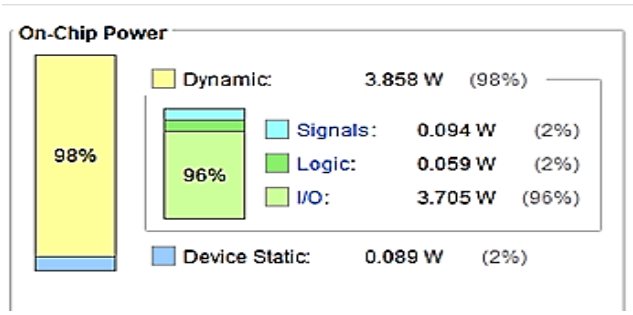

Figure 5: Power report of the system

E. Device Layout After Implementation

Figure 6 shows the device layout obtained after the implementation.

Figure 6: Device layout of the system

VI. CONCLUSION

The traffic light controller system is well suited to regulate traffic at four-way intersections. Verilog HDL is used for programming purposes because if the user wishes to make any changes in the system, it is possible to apply the required changes easily through Verilog HDL code.
The simulated waveform matched the traffic light signals obtained from the state table. The implemented system had a minimal power utilization of 3.948 W and used only 0.03% of the flip flops and 9.24% of the total IO (Input Output) facilities present in the FPGA.

VII. FUTURE WORK

As a future scope, cameras and sensors can be integrated into the designed system so that when the traffic controller system sees more traffic or more vehicles, it can automatically divert the traffic accordingly to ensure that there is no obstacle and the way for the vehicles is clear.

CONFLICTS OF INTEREST

The authors declare that they have no conflict of interest.

REFERENCES

1) Madras Institute of Technology Anna University Chennai, Department of Electronics Engineering, "International Journal of Advances in Engineering and Management (IJAEM)," vol. 4, no. 6, pp. 740-743, Jun. 2022. [Online]. Available: www.ijaem.net
2) Raj Kumar Goel Institute of Technology (RKGIT), Ghaziabad, Uttar Pradesh (201003), Department of Electronics and Communication Engineering, NBA Accredited.
3) S. B. B. Shabarinath and K. Swetha Reddy, "Timing and Synchronisation for explicit FSM based Traffic Light Controller," in IEEE 7th International Advance Computing Conference, 2017.
4) B. K. Koay and M. M. Isa, "Traffic Light System Design on FPGA," in Proceedings of 2009 IEEE Student Conference on Research and Development (SCOReD 2009), UPM Serdang, Malaysia, 16-18 Nov. 2009.
5) V. K. S. Venkata, "FPGA based Traffic Light Controller," in International Conference on Trends in Electronics (ICEI), 2017.
6) D. Bhavana et al., "Traffic Light Controller Using FPGA," International Journal of Engineering Research and Applications (IJERA), 2015.
7) W. M. E. Medany and Hussain, "FPGA based Advanced Real Traffic Light Controller System Design," in IEEE Workshop on Intelligent Data Acquisition Computing Systems: Technology and Applications, Germany, 2007.
8) S. Nath et al., "Design of an intelligent Traffic Light Controller with VHDL," in International Conference on Radar, Communication, and Computing, 2012, pp. 92-97.

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