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Multilevel Inverter Based Active Power Filter With Energy Balanced DC Link Capacitor

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Abstract—**This paper presents the modeling of a multilevel cascaded H-bridge inverter for a three phase shunt active power filter (APF). Multilevel-cascaded inverter can give better performance compared to other topologies. The DC link capacitor is designed based on energy balance principle. A closed loop current control technique is used to reduce harmonics and the voltage regulations are carried out by PI controller. The proposed modeling is verified by using MATLAB-Simulink software**

Keywords- **Active power filter; multilevel inverter; DC link capacitor; current controller.**

I. INTRODUCTION

Harmonic pollution is regarded as being one of the major problems that degrade electric power quality. Particularly, harmonic resonance in power distribution systems can cause excessive voltage and current waveforms distortion with a consecutive instability, abnormal operation or damage of electric components. The passive filter is sensitive to system impedance and load characteristics. The series and parallel resonance problems of this filter are hardly possible to be solved. Control of harmonic perturbations by active power filters (APF) has become a hot topic in the power engineering field. In the past two decades, active power filters have been developed to suppress harmonics generated by static power converters. Different active power filter configurations using series and shunt connections have been proposed and are recognized as viable solutions to the problems created by harmonic components [1].

Use of multilevel inverters in active power filters is the present research area. Several configurations of multilevel inverters have been proposed for the power stage of shunt active power filters, where the main objectives are tracking a reference current signal and maintain regulated dc voltages. In [2] and [3] a three-level neutral point clamped (NPC) inverter is used like a shunt active power filter.

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A cascaded H-bridge inverter is having better performance characteristics compared to other multilevel inverter topologies.

In this work a closed loop current controller is used to compensate the harmonic currents. The important technique in APF is to generate the reference current. The reference current will be generated using instantaneous real and reactive power theory. The major problem occurred in multilevel inverter based active power filter is the maintenance of DC link capacitor voltage. By using a PI controller we can make capacitor voltage as constant.

The main focus of this paper is, design of DC link capacitor and the inductor at common coupling point (CCP). The modelling is verified by using MATLAB-Simulink software.

II. MULTILEVEL INVERTER

The concept of multilevel converters has been introduced since 1975.The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed [4-6]. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform.

Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

Out of different multilevel inverter topologies, cascaded H-bridge inverter is more advantageous [7]. In cascaded h-bridge inverter, number of single phase inverters will be connected in series. The output voltage levels will be depended upon the number of converters connected in series

$$S = (2N + 1) \tag{1}$$

Where S= number of output voltage levels.
N= number of inverters connected in series.

For each single phase inverter, a DC link capacitor will be used to give the supply voltage. This DC link capacitor will be designed based on energy balanced principle. Fig1. Shows the basic structure of a multilevel inverter.

III. MULTILEVEL INVERTER BASED ACTIVE POWER FILTER

Fig2. Shows the block diagram of APF. Multilevel inverter will be connected in parallel with the load.

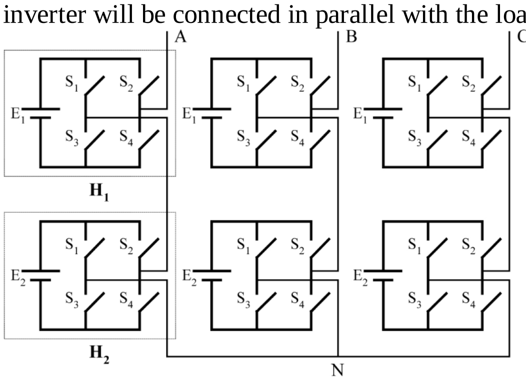

Fig1. Basic structure of a five level cascaded inverter

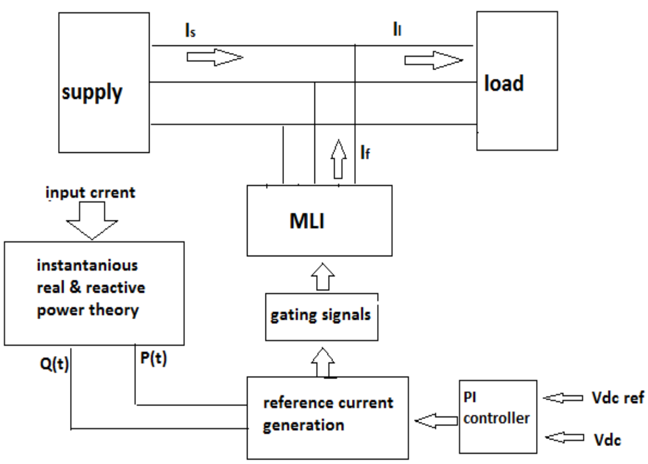

Fig 2. Block diagram of active power filter

By using P-Q theory, instantaneous real and reactive power will be generated. Important thing is to generate reference current for MLI. The reference current will depend upon the harmonics presented in the system current. The reference current signals will be given to the MLI controller, where the appropriate gating pulses will be generated. Carrier phase shifted PWM technique was used. In this technique to carrier signals which are phase shifted by some angle were used. Fig 3. Shows the simulink model of carrier phase shifted controller of a single phase.

IV. INSTANTANEOUS REAL AND REACTIVE POWER THEORY

By using P-Q theory, the instantaneous real and reactive power will be measured [8].

Source voltage and current will be converted into d-q coordinates.

$$P = V_\alpha I_\alpha + V_\beta I_\beta$$

$$Q = V_\alpha I_\beta - V_\beta I_\alpha$$

The measured real and reactive power will consists of both AC and DC quantities. DC quantities will be filtered using a low pass filter.

Now, by using inverse d-q transformation, the reference currents will be generated. Fig 4. Shows the reference current generated. These reference currents will be given to MLI controller.

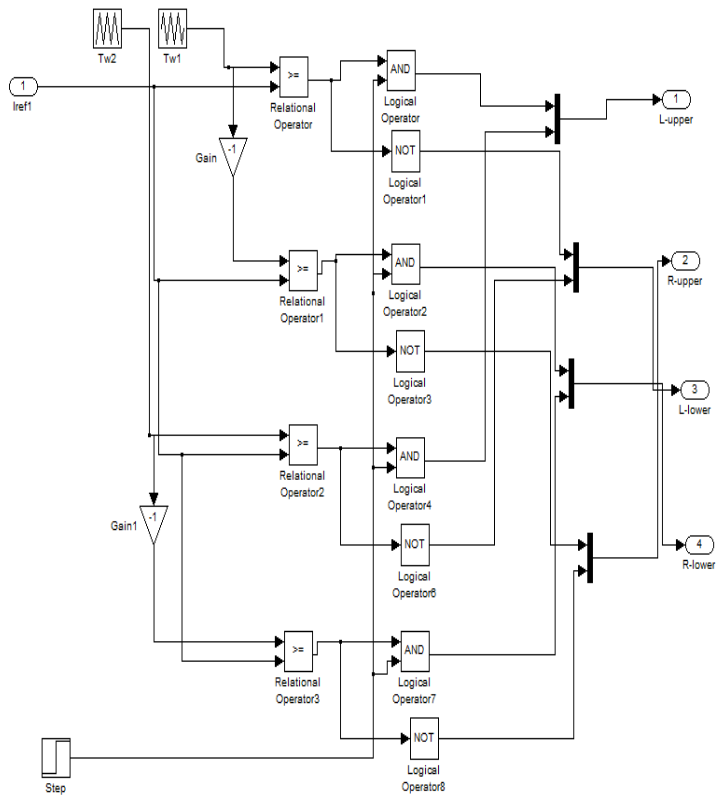

Fig 3. Carrier phase shifted PWM controller

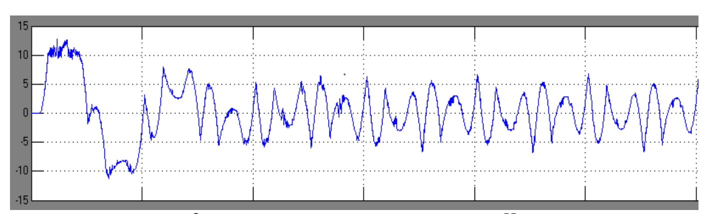

Fig 4. Reference current to MLI controller

The above shown reference current is of a single phase, there reference currents will be generated for three phases.

V. DESIGN OF DC LINK CAPACITOR

Design of DC link capacitor is based on the energy balance principle. DC link capacitor supplies or absorbs the energy whenever there is a sudden change in the active power demand by the load. Hence, DC link capacitor will be determined based on energy balance principle. Energy stored in capacitor is equal to energy demand of the load during transient. Thus,

$$\frac{1}{2}C(V_c^2 - V_{c,\min}^2) = V_s.I_s.\frac{T}{2} \quad (2)$$

Where C= DC link capacitance

$V_{c,\min} =$ Desired minimum capacitor voltage.

T = time period of the supply.

After simplification equation (2)

$$C = \frac{V_s..I_s.T}{(V_c^2 - V_{c,\min}^2)} \quad (3)$$

VI. MATHEMATICAL MODEL OF APF

A. Modeling of MLI

Fig 5. Shows the simulink model of active power filter. From this figure we can write

$$V_s = L_f \frac{di_{comp}}{dt} + R_f i_{comp} + sV_c$$

Or

$$\frac{di_{comp}}{dt} = \frac{V_s - R_f i_{comp} - sV_c}{L_f} \quad (4)$$

Where,

$V_s = V_m \sin \omega t =$ source voltage,

$L_f =$ Filter inductance,

$R_f =$ Resistance of the filter inductance,

$i_{comp} =$ Compensator current of the active filter,

$V_c =$ Voltage across the capacitor,

$s =$ Switching function,

The capacitor voltage is given by

$$\frac{dV_c}{dt} = \frac{si_{comp}}{C} \quad (5)$$

Solving equation (4) & (5)

The mathematical model of the converter can be expressed in terms of state space equation as

$$\frac{d}{dt}\begin{bmatrix} i_{comp} \\ V_c \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & -\frac{s}{L_f} \\ \frac{s}{C} & 0 \end{bmatrix} \begin{bmatrix} i_{comp} \\ V_s \end{bmatrix} + \begin{bmatrix} \frac{V_s}{L_f} \\ 0 \end{bmatrix} \quad (6)$$

Now the function of active power filter is to compensate the harmonic current, the magnitude of compensating current will be equal to the harmonic current but exactly in opposite phase.

$$I_l = I_s + i_{comp}$$

B. Filter inductance;

The design of filter inductance L_f is based on the current control technique used for generation of the switching pulse for the converter switches. In this work, carrier phase shifted PWM technique is used, in which two triangular signals will be compared with the generated reference signal.

Value of filter inductor is calculated with the constraint that for a given switching frequency the maximum slope of the inductor current shall be smaller than the slope of the triangular carrier waveform.

The slope of the triangular waveform, λ is defined as

$$\lambda = 4A_c f_c$$

Where $2A_c$ is peak to peak amplitude of the triangular waveform and f_c is the frequency of triangular carrier waveform.

The maximum permissible slope of the inductor current is given by

$$\frac{di_l}{dt} = \frac{V_s + V_c}{L}$$

Since the slope of the inductor current has to be smaller than the carrier triangular waveform, therefore

$$L_f \geq \frac{V_s + V_c}{4A_c f_c}$$

VII. SIMULATION RESULTS AND ANALYSIS

The simulation parameters for this work are as fallows

$V_s = 440$ Volts line to line, $V_{dc,ref} = 300$ volts,

$V_c = 300$ volts, $C = 2100\mu F$, $L_f = 2mH$

Fig 5 gives the current drawn by the nonlinear load is as fallows. As non linear load current consists of the harmonics, THD is given in fig 6.

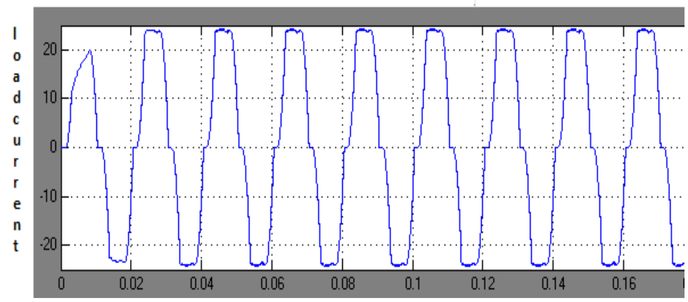

Fig 5 load current

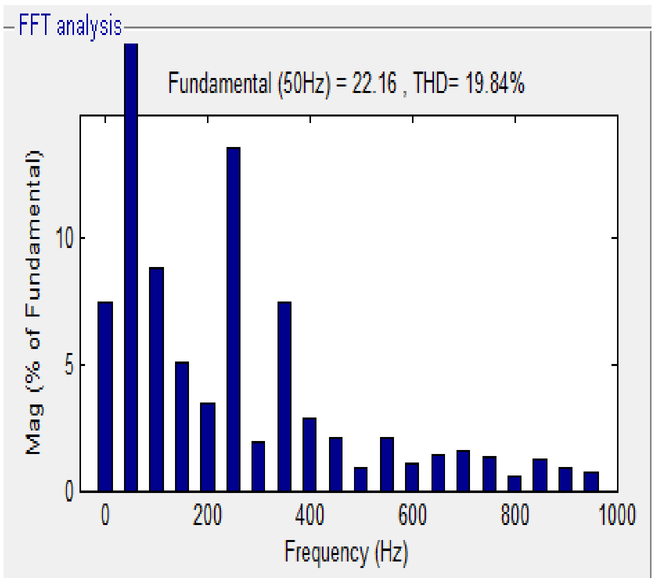

Fig 6 THD of load current

In order to reduce these harmonics and to improve the fundamental component at source end, the MLI is connected in parallel with the load at common coupling point (CCP). when the filter is initiated the source current will become free from harmonic components. Fig 7 shows the source current after filtering.

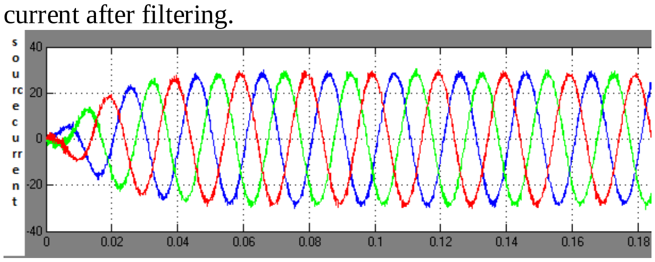

Fig 7 Three phase source current after filtering.

Now, the THD has been reduce to 1.98%and the fundamental component has been improved to 97.57%

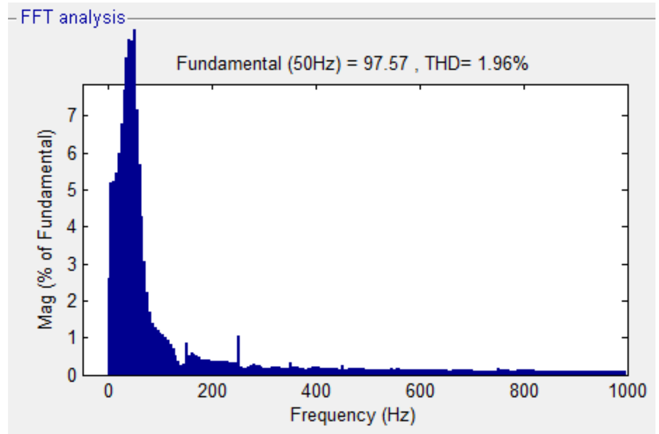

Fig 8 THD for source current

The important thing in APF is to maintain the capacitor voltage as constant. For this, the capacitor voltage will be compared with a reference voltage. The error signal will be processed through a PI controller. Fig 9 shows the capacitor voltage. From this figure we can observe the capacitor voltage is maintained constant at 300 volts.

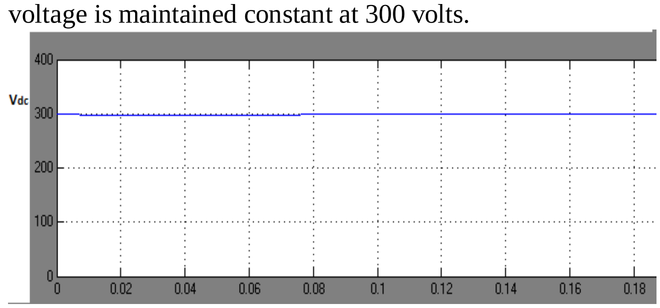

Fig 9 Capacitor voltage.

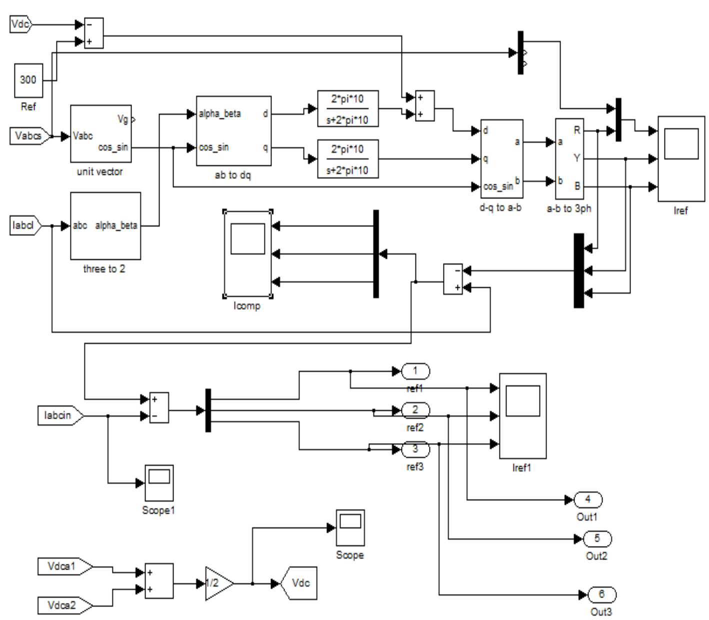

Fig 10 simulink diagram of current controller

VIII. CONCLUSION

In this paper cascade multilevel inverter based APF is implemented in high voltage system. This eliminates need of high cost transformer with APF in high voltage systems. Cascade type inverter has certain advantages as compared with other types and no separate Dc source is required. Carrier phase shifted PWM technique is used to reduce individual devices switching frequency. The DC link capacitor is designed based on energy balance principle. The voltage of the capacitor is maintained constant using a PI controller.

simulation results shows that multilevel inverter based active power filter can reduce the harmonics without the use of transformer. Total harmonic distortion has been improved.

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REFERENCES

[1] Singh B.,Haddead K., and Chandra A.,"A Review of active power filter for power quality improvement", IEEE Trans. Industrial Electronics, Vol.46 no.5,(1999):pp. 960-971.

[2] Mirinda H.,Cardenas V.,Visairo N.,Espinoza-perez G.,"A dq passivity based approach for shunt active power filter based onNPC three level converter" Industrial Electronics 34th annual conference of IEEE(2008):pp. 3171-3177.

[3] Three-level inverter based shunt active power filter in Three phase Three wireand four wire systems" IEEE trans. Volume:24(2009): pp. 1350-1363.

[4] Manjrekar M., Venkataramanan G.:"Advanced topologies and modulation strategies for multilevel inverters",PESC'96, volume:2(1996),pp:1013-1018.

[5] Rodriguez J.,Jih-sheng Lai, Fang Jeng Peng; "Multilevel inverter: a survey of topologies, controls and applications",IEEE trans. Volume: 49(2002), pp:724-738.

[6] Daher S.,Schmid J.,Antunes M.," Multilevel inverter topologies for stand alone PV systems"; IEEE trans. Volume:45(2008),pp: 2703-2712.

[7] Gupta R.,Ghosh A., Josh A.," switching characterization of cascaded multilevel inverter- controlled systems", IEEE trans. Volume: 55, year: 2008, pp: 1047-1058.

[8] Hafner J.,Aredes M.,Heumann K.," Ashunt active power filter applied to high voltage distribution line" IEEE trans. Power delivery., volume:12 (1997):pp:266-272.